Remarks

Claims 1, 2, and 4-23 are pending in this application. Claims 1, 5, 12, 17, 21 and 22 were previously amended. The Examiner has rejected claims 1, 2, and 4-23 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,017,054 to Schuckle et al, (hereinafter "Schuckle").

1. Rejections under 35 U.S.C. 102(e)

The Examiner has rejected claims 1, 2, and 4-23 as being anticipated by Schuckle. A prior art patent, publication or event is for the same "invention," as that word is used in §102, and therefore anticipating, if the prior art patent, publication or event discloses each and every limitation found in the claims, either expressly or inherently. Rockwell Intern. Corp. v. U.S., 147 F.3d 1358, 1363 (Fed. Cir. 1998); Electro Med. Sys. S.A. v. Cooper Life Sciences, 34 F.3d 1048, 1052 (Fed. Cir. 1994). Each claim limitation must be found in a single prior art reference; references cannot be combined under §102. Apple Computer, Inc. v. Articulate Systems, Inc., 234 F.3d 14, 20 (Fed. Cir. 2000). Omission of any claimed element, no matter how insubstantial, is grounds for traversing a rejection based on §102. Connell v. Sears, Roebuck & Co., 722 F.2d 1542 (Fed. Cir. 1983).

Schuckle fails to disclose each and every limitation found in independent claims 1, 5, 12, 17, and 21. Specifically, Schuckle does not teach the **invalidation** of those lines in the cache corresponding to the **entries of the write tracking buffer** (upon the processor exiting its low power state).

In the system and methods of the present invention, when the processor exits the low power state, the processor invalidates in its internal cache those cache lines that correspond to the addresses recorded in the write-tracking buffer. (Spec., Abstract and Figure 3) This

process insures coherence between the processor's internal cache and the system memory of the computer system, while allowing for the management of power conservation. (Spec., [0007])

In contrast to the system and methods of the present invention, Schuckle does not teach the invalidation of those lines in the cache corresponding to the entries of the write-tracking buffer (which keeps track of writes during the low power state). The Examiner points to column 6 and 7 of Schuckle as teaching this element. (Office Action, p.3-5) The cited portions of Schuckle fail to discuss the invalidation of cache lines upon exit from a low power state; at best, the cited portions discuss snooping and the snoopable power state. (Schuckle, col. 6-7) When Schuckle does discuss invalidation, it is specifically with respect to performing cache tag invalidates for all *unmodified* cache lines. (Schuckle, Figure 3B, 3406) Schuckle states, "If the cache line has not been modified, i.e., is *unmodified*, then processor 110 remains in a lower power state, provided the cache line is *invalidated* upon the processor returning to the appropriate power state." (Schuckle, col. 11, lines 45-50, emphasis added) Schuckle does not disclose the invalidation of those lines in the cache corresponding to the entries of a write tracking buffer.

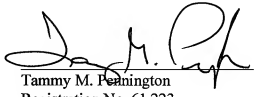
Because Schuckle does not teach all of the elements of the independent claims, Applicant respectfully requests that the rejection of independent claims 1, 5, 12, 17, and 21 be withdrawn and contend that these claims are in condition for allowance.

Dependent claims 2, 4, 6-11, 13-16, 18-20, and 22-23 will not be individually discussed herein because they stem from otherwise allowable base claims.

Conclusion

Applicant respectfully submits that pending claims 1, 2, and 4-23 of the present invention, as amended, are allowable. Applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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